Claims

What is claimed is:

1. An electronic apparatus comprising:

a first integrated circuit semiconductor die comprising:

a first signal conditioning circuit integrated within the first integrated circuit die for performing a first signal conditioning function on a signal propagating along a first signal path;

a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first signal conditioning circuit for other than performing the first signal conditioning function and for use by the first signal conditioning circuit during operation thereof;

a second integrated circuit semiconductor die comprising a second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path;

a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second signal conditioning circuit for other than performing the second signal conditioning function and for use by the second signal conditioning circuit during operation thereof;

a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

2. An electronic apparatus according to claim 1, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning operations.

3. An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon based technology.

4. An electronic apparatus according to claim 3, wherein the second integrated circuit die is manufactured using a second semiconductor process and utilizes an other than silicon based technology.

5. An electronic apparatus according to claim 1, wherein the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

6. An electronic apparatus according to claim 1, wherein the second signal conditioning circuit comprises at least a power amplifier circuit and where the function of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

7. An electronic apparatus according to claim 1, wherein the second semiconductor process does not facilitate manufacturing and integration of the second ancillary circuit therein.

8. An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.

9. An electronic apparatus according to claim 5, wherein the first ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry.

10. An electronic apparatus according to claim 6, wherein the second ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry.

11. An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

12. An electronic apparatus according to claim 11, wherein the second integrated circuit die is derived from a second semiconductor wafer the other one of Si, SiGe, GaAs, InP, and GaN.

13. An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a BiCMOS process.

14. An electronic apparatus according to claim 13, wherein the first integrated circuit die comprises SiGe.

15. An electronic apparatus according to claim 1, wherein the first integrated circuit die comprises a first interface port connected to the second ancillary circuit and wherein the second integrated circuit die comprises a second interface port connected to the second signal conditioning circuit, the second signal conditioning circuit for being connected to the second ancillary circuit using the first and second interface ports.

16. An electronic apparatus according to claim 1, wherein the second signal conditioning circuit is for performing the second signal conditioning function in conjunction with operation of the second ancillary circuit.

17. An electronic apparatus comprising:

a first integrated circuit die formed using a first semiconductor process, the first integrated circuit die other than requiring additional circuitry for use in performing a first signal conditioning function comprising:

a first signal conditioning circuit for performing the first signal conditioning function and having a first input port for receiving a first input signal

for performing the first signal conditioning function thereon and having a first output port for providing a first output signal therefrom;

a first ancillary circuit electrically coupled to the first signal conditioning circuit for use by the first signal conditioning circuit during operation thereof;

a second ancillary circuit having a first interface port; and,

a second integrated circuit die formed using a second semiconductor process and having a second input port for receiving a second input signal, and a second output port for providing a second output signal therefrom, the second integrated circuit die having a second interface port for interfacing with the first interface port for performing a second signal conditioning function in conjunction with the second ancillary circuit disposed on the first integrated circuit die with no signal communication occurring between the first and second input ports and between the first and second output ports.

18. An electronic apparatus according to claim 17, wherein the second integrated circuit die cannot provide the second function without operation of the second ancillary circuit.

19. An electronic apparatus according to claim 17, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning operations.

20. An electronic apparatus according to claim 17, wherein the first integrated circuit die is manufactured using a silicon based technology.

21. An electronic apparatus according to claim 20, wherein the second integrated circuit die is manufactured using other than silicon based technology.

22. An electronic apparatus according to claim 17, wherein at least one of the first signal conditioning circuit and the second signal conditioning circuit comprises at least a power amplifier circuit.

23. An electronic apparatus according to claim 17, wherein the first ancillary circuit and the second ancillary circuit each comprises at least one of voltage regulation circuitry and temperature control circuitry.

24. An electronic apparatus according to claim 23, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

25. An electronic apparatus according to claim 17, wherein the first integrated circuit die is manufactured using a BiCMOS process.

26. An electronic apparatus according to claim 17, comprising a module substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

27. A method of manufacturing a circuit for reducing crosstalk comprising the steps of:

providing a first signal conditioning circuit;

providing a second signal conditioning circuit;

implementing the first signal conditioning circuit within a first semiconductor die;

implementing a first portion of the second signal conditioning circuit in the first semiconductor die;

implementing a second portion of the second signal conditioning circuit in a second semiconductor die;

bonding the first and second dies to a common substrate; and,

wire bonding between the two dies to complete the second signal conditioning circuit.

28. A method according to claim 27, wherein the first semiconductor die comprises a first signal path.

29. A method according to claim 28, wherein the second semiconductor die comprises a second signal path that is other than the first signal path and in approximate RF isolation therefrom.

30. A method according to claim 27, wherein the second semiconductor die is manufactured using a more expensive semiconductor process than that used for manufacturing of the first semiconductor die.

31. A method according to claim 27, wherein the first portion of the second signal conditioning circuit is more cost effectively implemented in the first semiconductor die.

32. A method according to claim 27, wherein prior to the step of implementing the first portion of the second signal conditioning circuit in the first semiconductor die, comprises the step of partitioning of the second signal conditioning circuit into the first portion and the second portion.